DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD441000L-X

1M-BIT CMOS STATIC RAM
128K-WORD BY 8-BIT
EXTENDED TEMPERATURE OPERATION

Description

The μPD441000L-X is a high speed, low power, 1,048,576 bits (131,072 words by 8 bits) CMOS static RAM.

The μPD441000L-X has two chip enable pins (/CE1, CE2) to extend the capacity.

★ The μPD441000L-X is packed in 32-pin plastic SOP, 32-pin plastic TSOP (I) and 36-pin plastic FPBGA.

Features

- 131,072 words by 8 bits organization
- Fast access time: 70, 85, 100, 120, 150 ns (MAX.)
- Low voltage operation (B version: V_{CC} = 2.7 to 3.6 V, C version: V_{CC} = 2.2 to 3.6 V, D version: V_{CC} = 1.8 to 3.6 V)
- Operating ambient temperature: T_A = –25 to +85 °C
- Output Enable input for easy application
- Two Chip Enable inputs: /CE1, CE2

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current		
				At operating mA (MAX.)	At standby μA (MAX.)	At data retention μA (MAX.)
μPD441000L-BxxX	70, 85, 100	2.7 to 3.6	–25 to +85	25	2	2
μPD441000L-CxxX	100, 120	2.2 to 3.6				
μPD441000L-DxxX	120, 150	1.8 to 3.6				

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The mark ★ shows major revised points.

Ordering Information

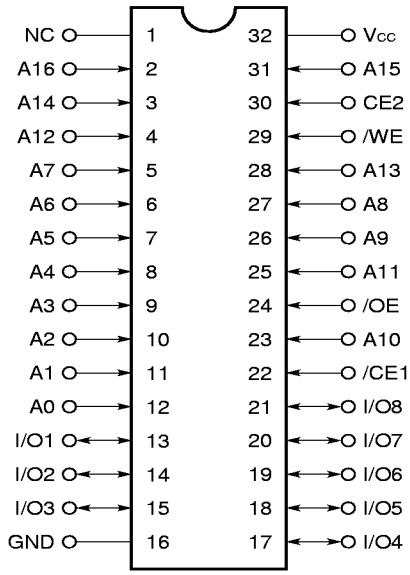
Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating Temperature °C	Remark
★ μPD441000LGW-B70X	32-pin Plastic SOP (525 mil)	70	2.7 to 3.6	–25 to +85	B Version
★ μPD441000LGW-B85X		85			
★ μPD441000LGW-B10X		100			
★ μPD441000LGW-C10X		100	2.2 to 3.6		C Version
★ μPD441000LGW-C12X		120			
★ μPD441000LGW-D12X		120	1.8 to 3.6		D Version
★ μPD441000LGW-D15X		150			
μPD441000LGU-B70X-9JH	32-pin Plastic TSOP (I)	70	2.7 to 3.6		B Version
μPD441000LGU-B85X-9JH	(8 x 13.4 mm) (Normal bent)	85			
μPD441000LGU-B10X-9JH		100			
μPD441000LGU-C10X-9JH		100	2.2 to 3.6		C Version
μPD441000LGU-C12X-9JH		120			
μPD441000LGU-D12X-9JH		120	1.8 to 3.6		D Version
μPD441000LGU-D15X-9JH		150			
μPD441000LGU-B70X-9KH	32-pin Plastic TSOP (I)	70	2.7 to 3.6		B Version
μPD441000LGU-B85X-9KH	(8 x 13.4 mm) (Reverse bent)	85			
μPD441000LGU-B10X-9KH		100			
μPD441000LGU-C10X-9KH		100	2.2 to 3.6		C Version
μPD441000LGU-C12X-9KH		120			
μPD441000LGU-D12X-9KH		120	1.8 to 3.6		D Version
μPD441000LGU-D15X-9KH		150			
μPD441000LGZ-B70X-KJH	32-pin Plastic TSOP (I)	70	2.7 to 3.6		B Version
μPD441000LGZ-B85X-KJH	(8 x 20 mm) (Normal bent)	85			
μPD441000LGZ-B10X-KJH		100			
μPD441000LGZ-C10X-KJH		100	2.2 to 3.6		C Version
μPD441000LGZ-C12X-KJH		120			
μPD441000LGZ-D12X-KJH		120	1.8 to 3.6		D Version
μPD441000LGZ-D15X-KJH		150			
μPD441000LGZ-B70X-KKH	32-pin Plastic TSOP (I)	70	2.7 to 3.6		B Version
μPD441000LGZ-B85X-KKH	(8 x 20 mm) (Reverse bent)	85			
μPD441000LGZ-B10X-KKH		100			
μPD441000LGZ-C10X-KKH		100	2.2 to 3.6		C Version
μPD441000LGZ-C12X-KKH		120			
μPD441000LGZ-D12X-KKH		120	1.8 to 3.6		D Version
μPD441000LGZ-D15X-KKH		150			
★ μPD441000LF1-BA1-B70X Note	36-pin Plastic FPBGA	70	2.7 to 3.6		B Version
★ μPD441000LF1-BA1-B85X Note	(6.0 x 6.0 mm)	85			
★ μPD441000LF1-BA1-B10X Note		100			
★ μPD441000LF1-BA1-C10X Note		100	2.2 to 3.6		C Version
★ μPD441000LF1-BA1-C12X Note		120			
★ μPD441000LF1-BA1-D12X Note		120	1.8 to 3.6		D Version
★ μPD441000LF1-BA1-D15X Note		150			

★ **Note** Under development

Pin Configuration (Marking Side)

/xxx indicates active low signal.

★ **32-pin Plastic SOP (525 mil)**
[μPD441000LGW-BxxX]
[μPD441000LGW-CxxX]
[μPD441000LGW-DxxX]



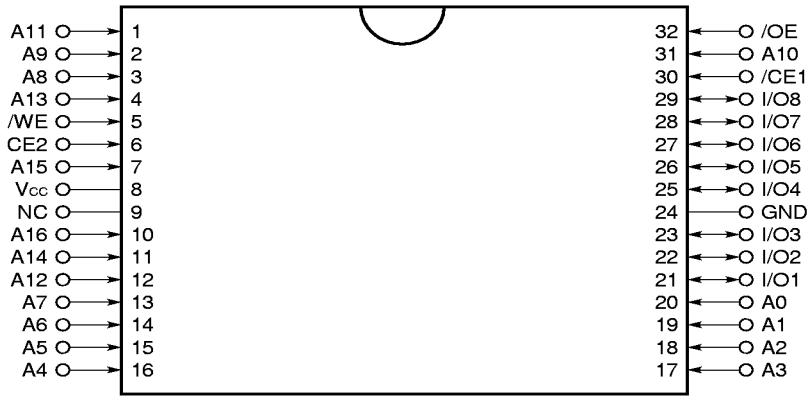
A0 - A16	:	Address inputs
I/O1 - I/O8	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
Vcc	:	Power supply
GND	:	Ground
NC	:	No connection

32-pin Plastic TSOP (I) (8 x 13.4 mm) (Normal bent)

[μPD441000LGU-BxxX-9JH]

[μPD441000LGU-CxxX-9JH]

[μPD441000LGU-DxxX-9JH]

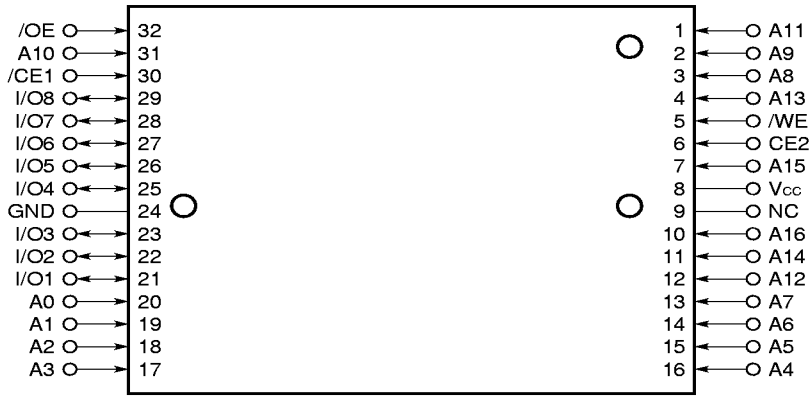


32-pin Plastic TSOP (I) (8 x 13.4 mm) (Reverse bent)

[μPD441000LGU-BxxX-9KH]

[μPD441000LGU-CxxX-9KH]

[μPD441000LGU-DxxX-9KH]



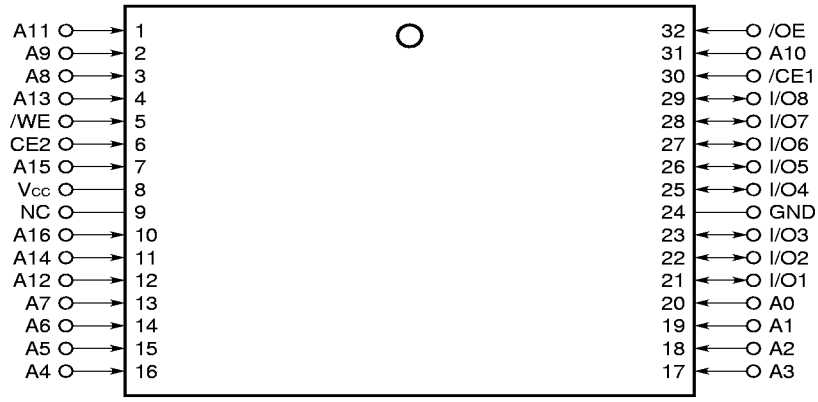
A0 - A16	:	Address inputs
I/O1 - I/O8	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
Vcc	:	Power supply
GND	:	Ground
NC	:	No connection

32-pin Plastic TSOP (I) (8 x 20 mm) (Normal bent)

[μPD441000LGZ-BxxX-KJH]

[μPD441000LGZ-CxxX-KJH]

[μPD441000LGZ-DxxX-KJH]

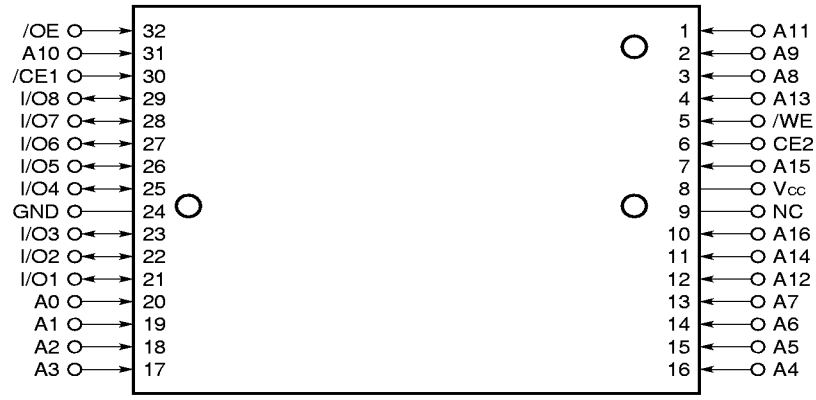


32-pin Plastic TSOP (I) (8 x 20 mm) (Reverse bent)

[μPD441000LGZ-BxxX-KKH]

[μPD441000LGZ-CxxX-KKH]

[μPD441000LGZ-DxxX-KKH]



A0 - A16	:	Address inputs
I/O1 - I/O8	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
Vcc	:	Power supply
GND	:	Ground
NC	:	No connection

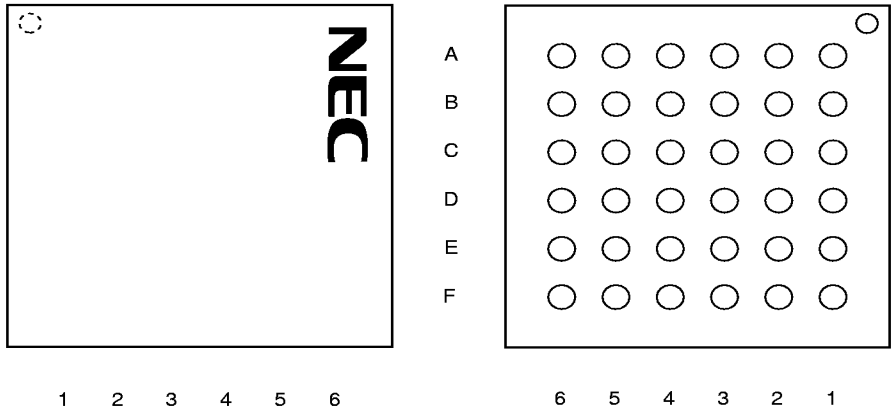
36-pin Plastic FPBGA (6.0 x 6.0 mm)

[μPD441000LF1-BA1-BxxX]

[μPD441000LF1-BA1-CxxX]

[μPD441000LF1-BA1-DxxX]

Top View **Bottom View**



Top view

	1	2	3	4	5	6
A	A7	CE2	Vcc	A15	A13	A11
B	A6	/WE	A16	IC	A8	A9
C	A3	A5	IC	IC	A12	A14
D	/OE	A0	IC	IC	A1	A4
E	/CE1	I/O3	I/O5	I/O6	I/O8	A2
F	I/O1	I/O2	I/O4	GND	I/O7	A10

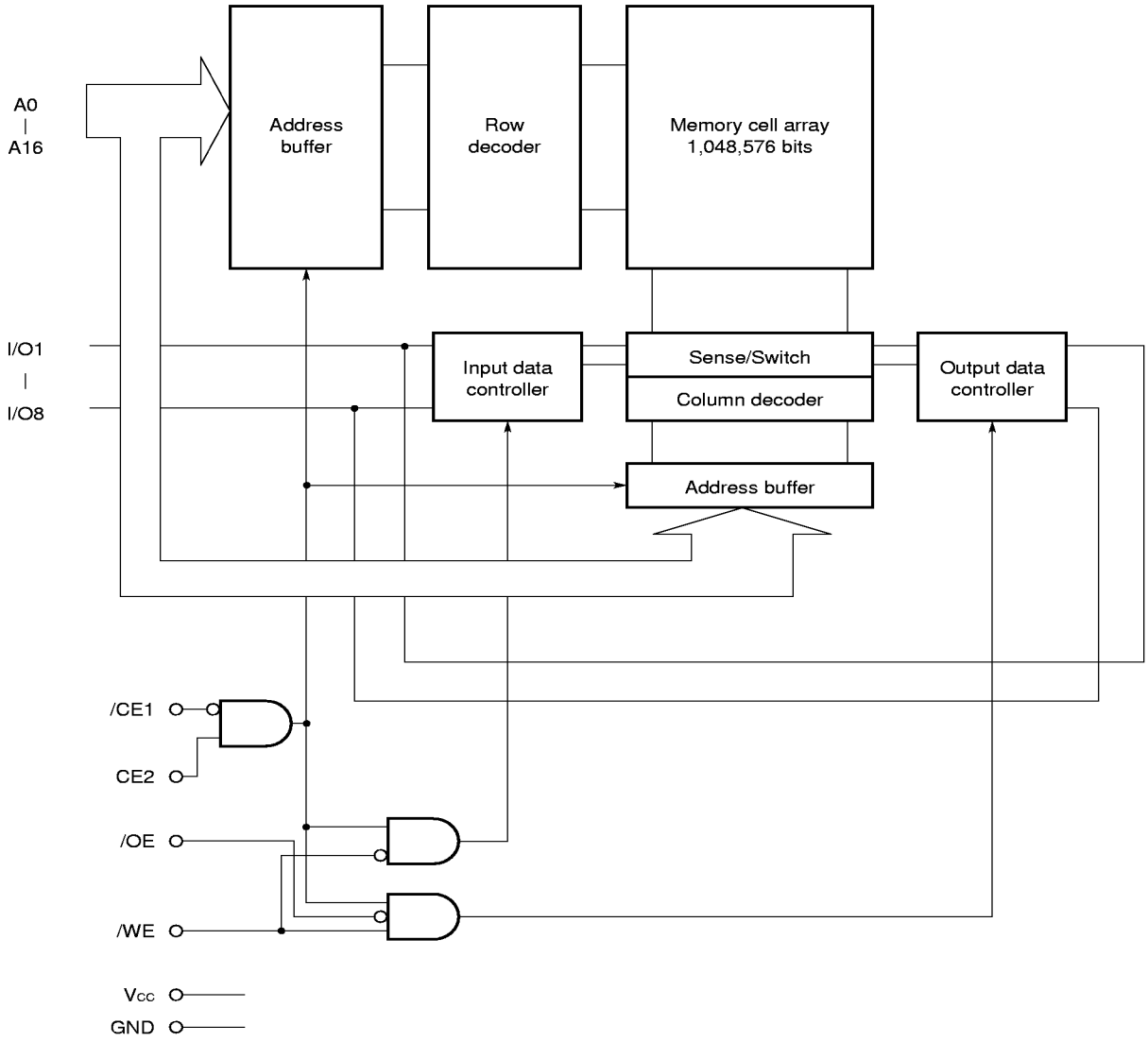
Bottom view

	6	5	4	3	2	1
A	A11	A13	A15	Vcc	CE2	A7
B	A9	A8	IC	A16	/WE	A6
C	A14	A12	IC	IC	A5	A3
D	A4	A1	IC	IC	A0	/OE
E	A2	I/O8	I/O6	I/O5	I/O3	/CE1
F	A10	I/O7	GND	I/O4	I/O2	I/O1

A0 - A16 : Address inputs
I/O1 - I/O8 : Data inputs / outputs
/CE1, CE2 : Chip Enable 1, 2
/WE : Write Enable
/OE : Output Enable
VCC : Power supply
GND : Ground
IC[Note] : Internal Connection

Note Leave this pin unconnected or connect to GND.

Block Diagram



Truth Table

/CE1	CE2	/OE	/WE	Mode	I/O	Supply current
H	×	×	×	Not selected	High impedance	I_{SB}
×	L	×	×			
L	H	H	H	Output disable		I_{CCA}
L	H	L	H	Read	D_{OUT}	
L	H	×	L	Write	D_{IN}	

Remark ×: Don't care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.5 Note to +4.6	V
Input / Output voltage	V_T		–0.5 Note to V_{CC}+0.5	V
Operating ambient temperature	T_A		–25 to +85	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –3.0 V (MIN.) (Pulse width: 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	μPD441000L-BxxX		μPD441000L-CxxX		μPD441000L-DxxX		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}		2.7	3.6	2.2	3.6	1.8	3.6	V
High level input voltage	V_{IH}	2.7 V ≤ V_{CC} ≤ 3.6 V	2.4	V_{CC}+0.5	2.4	V_{CC}+0.5	2.4	V_{CC}+0.5	V
		2.2 V ≤ V_{CC} < 2.7 V	–	–	2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	
		1.8 V ≤ V_{CC} < 2.2 V	–	–	–	–	1.6	V_{CC}+0.5	
Low level input voltage	V_{IL}		–0.3 Note	+0.5	–0.3 Note	+0.3	–0.3 Note	+0.2	V
Operating ambient temperature	T_A		–25	+85	–25	+85	–25	+85	°C

Note –3.0 V (MIN.) (Pulse width: 30 ns)

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition		μPD441000L-BxxX			μPD441000L-CxxX			μPD441000L-DxxX			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		−1.0		+1.0	−1.0		+1.0	−1.0		+1.0	μA
I/O leakage current	I_{LO}	V_{IO} = 0 V to V_{CC}, /CE1 = V_{IH} or CE2 = V_{IL} or /WE = V_{IL} or /OE = V_{IH}		−1.0		+1.0	−1.0		+1.0	−1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CE1 = V_{IL}, CE2 = V_{IH},			23	25		23	25		23	25	mA
		Minimum cycle time, $I_{I/O}$ = 0 mA	$V_{CC} \leq 2.7$ V		—	—		20	23		20	23	
			$V_{CC} \leq 2.2$ V		—	—		—	—		17	20	
	I_{CCA2}	/CE1 = V_{IL}, CE2 = V_{IH},				5			5			5	
		$I_{I/O}$ = 0 mA	$V_{CC} \leq 2.7$ V			—			4			4	
			$V_{CC} \leq 2.2$ V			—			—			3	
	I_{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V_{CC} − 0.2 V,				4			4			4	
		Cycle = 1 MHz, $I_{I/O}$ = 0 mA,	$V_{CC} \leq 2.7$ V			—			3			3	
		V_{IL} ≤ 0.2 V, V_{IH} ≥ V_{CC} − 0.2 V	$V_{CC} \leq 2.2$ V			—			—			3	
Standby supply current	I_{SB}	/CE1 = V_{IH} or CE2 = V_{IL}				0.3			0.3			0.3	mA
	I_{SB1}	/CE1 ≥ V_{CC} − 0.2 V,			0.05	2		0.05	2		0.05	2	μA
		CE2 ≥ V_{CC} − 0.2 V	$V_{CC} \leq 2.7$ V		—	—		0.04	2		0.04	2	
			$V_{CC} \leq 2.2$ V		—	—		—	—		0.03	1.5	
	I_{SB2}	CE2 ≤ 0.2 V			0.05	2		0.05	2		0.05	2	
			$V_{CC} \leq 2.7$ V		—	—		0.04	2		0.04	2	
			$V_{CC} \leq 2.2$ V		—	—		—	—		0.03	1.5	
High level output voltage	V_{OH}	I_{OH} = −0.5 mA		2.4			2.4			2.4			V
			$V_{CC} \leq 2.7$ V	—			1.8			1.8			
			$V_{CC} \leq 2.2$ V	—			—			1.5			
Low level output voltage	V_{OL}	I_{OL} = +1.0 mA				0.4			0.4			0.4	V

Remarks 1. V_{IN}: Input voltage

2. These DC characteristics are in common regardless of package types and access time.

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			6	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remarks 1. V_{IN}: Input voltage

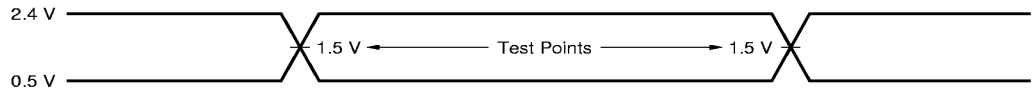
2. These parameters are periodically sampled and not 100% tested.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Test Conditions

μPD441000L-B70X, μPD441000L-B85X, μPD441000L-B10X

Input Waveform (Rise and Fall Time ≤ 5 ns)



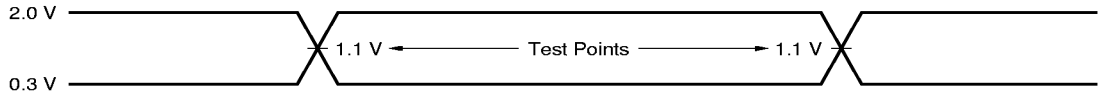
Output Waveform

Output Load

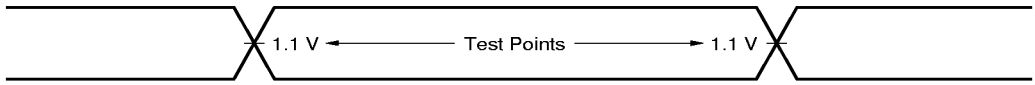
1TTL + 50pF

μPD441000L-C10X, μPD441000L-C12X

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

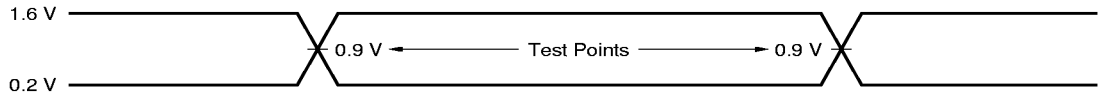


Output Load

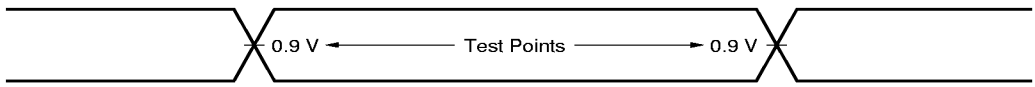
1TTL + 30pF

μPD441000L-D12X, μPD441000L-D15X

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

1TTL + 30pF

Read Cycle (1/3) (B version)

Parameter	Symbol	μPD441000L-B70X		μPD441000L-B85X		μPD441000L-B10X		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		85		100		ns	
Address access time	t_{AA}		70		85		100	ns	1
/CE1 access time	t_{CO1}		70		85		100	ns	
CE2 access time	t_{CO2}		70		85		100	ns	
/OE to output valid	t_{OE}		35		45		50	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		10		ns	2
CE2 to output in low impedance	t_{LZ2}	10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/CE1 to output in high impedance	t_{HZ1}		25		30		35	ns	
CE2 to output in high impedance	t_{HZ2}		25		30		35	ns	
/OE to output hold in high impedance	t_{OHZ}		25		30		35	ns	

Notes 1. See the output load.

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle (2/3) (C version)

Parameter	Symbol	μPD441000L-C10X		μPD441000L-C12X		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	100		120		ns	
Address access time	t_{AA}		100		120	ns	1
/CE1 access time	t_{CO1}		100		120	ns	
CE2 access time	t_{CO2}		100		120	ns	
/OE to output valid	t_{OE}		50		60	ns	
Output hold from address change	t_{OH}	10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		ns	2
CE2 to output in low impedance	t_{LZ2}	10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		ns	
/CE1 to output in high impedance	t_{HZ1}		35		40	ns	
CE2 to output in high impedance	t_{HZ2}		35		40	ns	
/OE to output hold in high impedance	t_{OHZ}		35		40	ns	

Notes 1. See the output load.

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle (3/3) (D version)

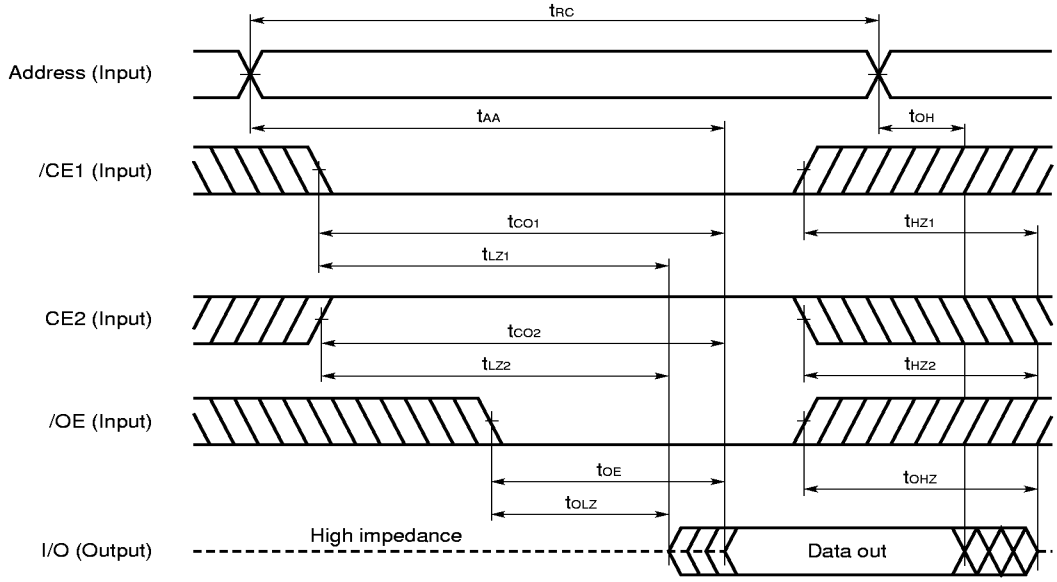
Parameter	Symbol	μPD441000L-D12X		μPD441000L-D15X		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	120		150		ns	
Address access time	t_{AA}		120		150	ns	1
/CE1 access time	t_{CO1}		120		150	ns	
CE2 access time	t_{CO2}		120		150	ns	
/OE to output valid	t_{OE}		60		70	ns	
Output hold from address change	t_{OH}	10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		ns	2
CE2 to output in low impedance	t_{LZ2}	10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		ns	
/CE1 to output in high impedance	t_{HZ1}		40		50	ns	
CE2 to output in high impedance	t_{HZ2}		40		50	ns	
/OE to output hold in high impedance	t_{OHZ}		40		50	ns	

Notes 1. See the output load.

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

Write Cycle (1/3) (B version)

Parameter	Symbol	μPD441000L-B70X		μPD441000L-B85X		μPD441000L-B10X		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		85		100		ns	
/CE1 to end of write	t_{CW1}	55		70		80		ns	
CE2 to end of write	t_{CW2}	55		70		80		ns	
Address valid to end of write	t_{AW}	55		70		80		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	50		60		60		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	35		35		40		ns	
Data hold time	t_{DH}	0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		25		30		35	ns	1
Output active from end of write	t_{OW}	5		5		5		ns	

Note 1. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Write Cycle (2/3) (C version)

Parameter	Symbol	μPD441000L-C10X		μPD441000L-C12X		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	100		120		ns	
/CE1 to end of write	t_{CW1}	80		100		ns	
CE2 to end of write	t_{CW2}	80		100		ns	
Address valid to end of write	t_{AW}	80		100		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	60		85		ns	
Write recovery time	t_{WR}	0		0		ns	
Data valid to end of write	t_{DW}	45		60		ns	
Data hold time	t_{DH}	0		0		ns	
/WE to output in high impedance	t_{WHZ}		35		40	ns	1
Output active from end of write	t_{OW}	5		5		ns	

Note 1. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

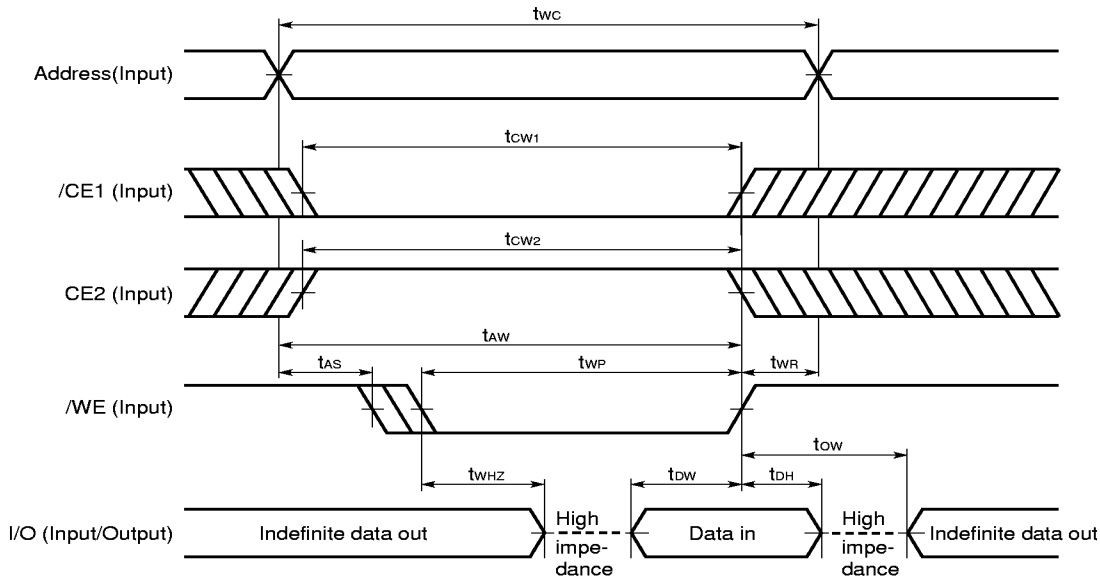
Write Cycle (3/3) (D version)

Parameter	Symbol	μPD441000L-D12X		μPD441000L-D15X		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	120		150		ns	
/CE1 to end of write	t_{CW1}	100		120		ns	
CE2 to end of write	t_{CW2}	100		120		ns	
Address valid to end of write	t_{AW}	100		120		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	85		100		ns	
Write recovery time	t_{WR}	0		0		ns	
Data valid to end of write	t_{DW}	60		80		ns	
Data hold time	t_{DH}	0		0		ns	
/WE to output in high impedance	t_{WHZ}		40		50	ns	1
Output active from end of write	t_{OW}	5		5		ns	

Note 1. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Write Cycle Timing Chart 1 (/WE Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

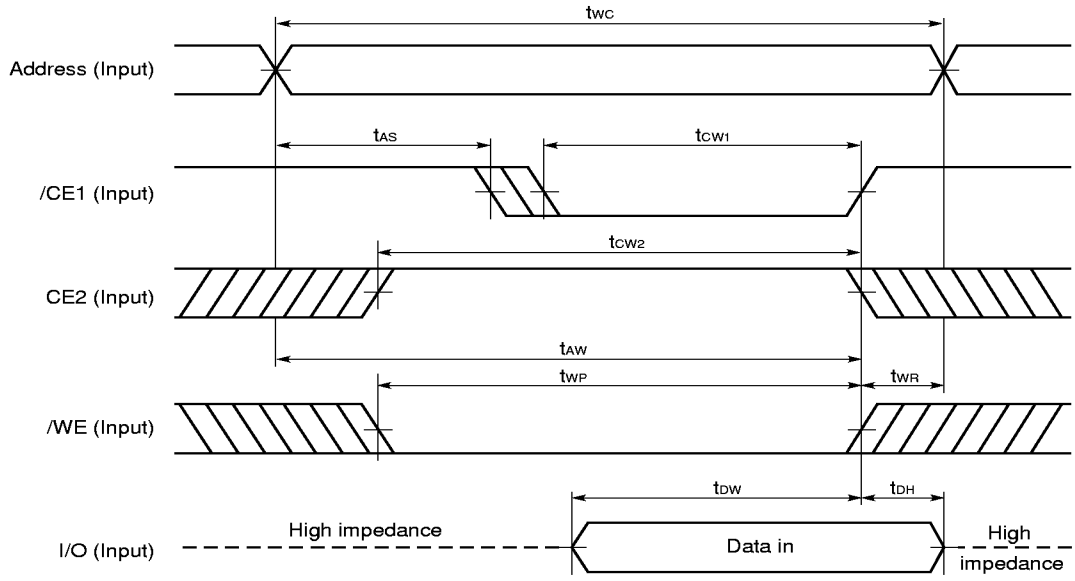
2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remarks 1. Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.

2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.

3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CE1 Controlled)

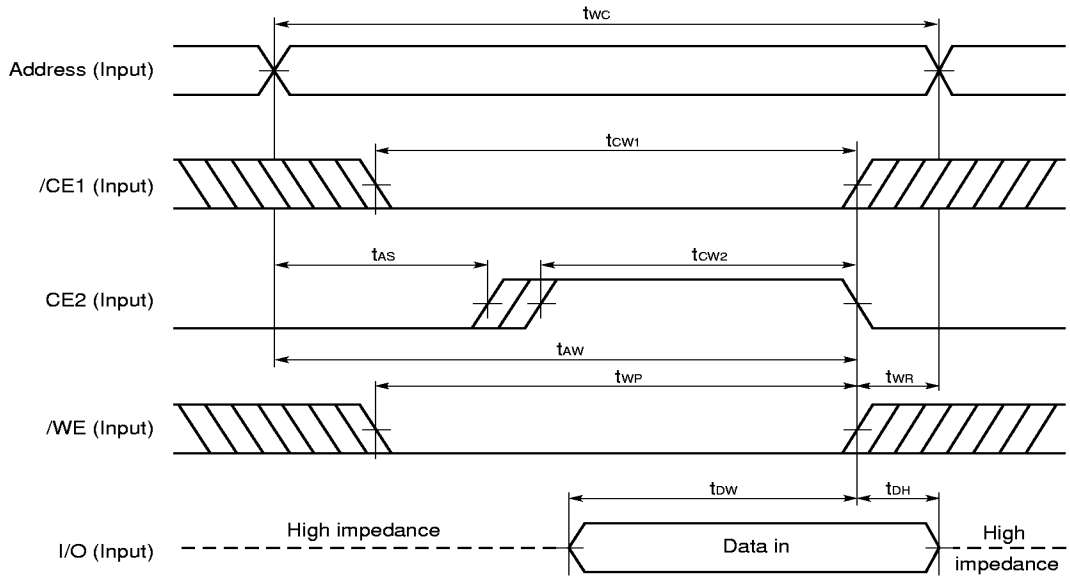


Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.

Low V_{CC} Data Retention Characteristics

B Version (μPD441000L-BxxX: T_A = –25 to +85 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{CCDR1}	/CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2V	2		3.6	V
	V_{CCDR2}	CE2 ≤ 0.2 V	2		3.6	
Data retention supply current	I_{CCDR1}	V_{CC} = 3.0 V, /CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V or CE2 ≤ 0.2 V		0.05	2 Note	μA
	I_{CCDR2}	V_{CC} = 3.0 V, CE2 ≤ 0.2 V		0.05	2 Note	
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		5			ms

Note 0.5 μA (T_A ≤ 40 °C)

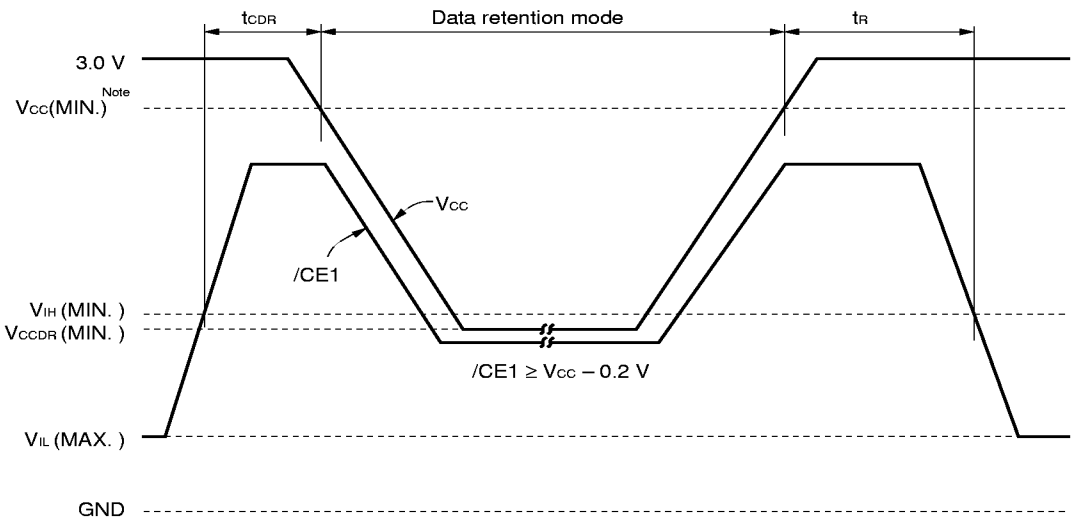
C, D Version (μPD441000L-CxxX, μPD441000L-DxxX: T_A = –25 to +85 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{CCDR1}	/CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2V	1.5		3.6	V
	V_{CCDR2}	CE2 ≤ 0.2 V	1.5		3.6	
Data retention supply current	I_{CCDR1}	V_{CC} = 3.0 V, /CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V or CE2 ≤ 0.2 V		0.05	2 Note	μA
	I_{CCDR2}	V_{CC} = 3.0 V, CE2 ≤ 0.2 V		0.05	2 Note	
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		5			ms

Note 0.5 μA (T_A ≤ 40 °C)

Data Retention Timing Chart

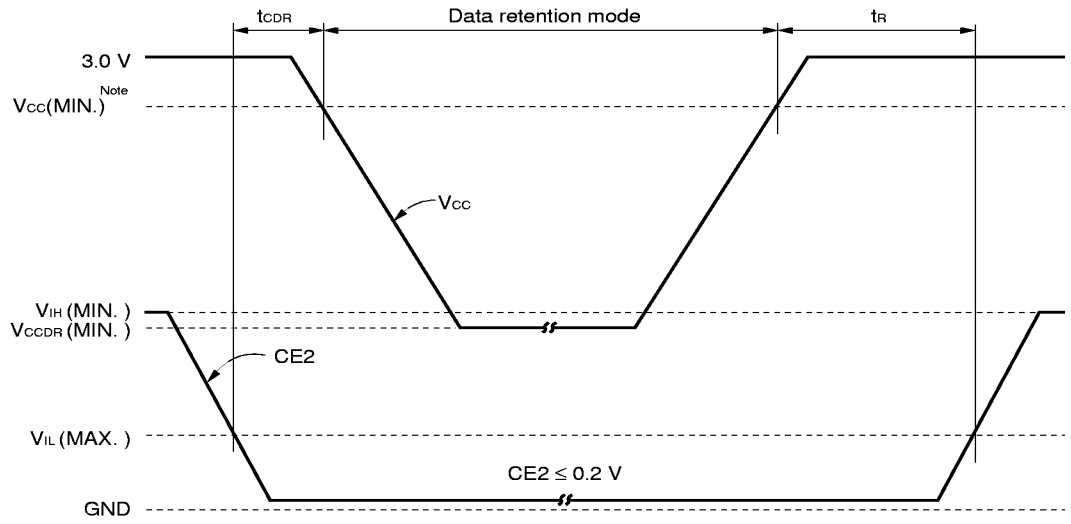
(1) /CE1 Controlled



Note B version: 2.7 V, C version: 2.2 V, D version: 1.8 V

Remark On the data retention mode by controlling /CE1, the input level of CE2 must be CE2 ≥ VCC – 0.2 V or CE2 ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

(2) CE2 Controlled

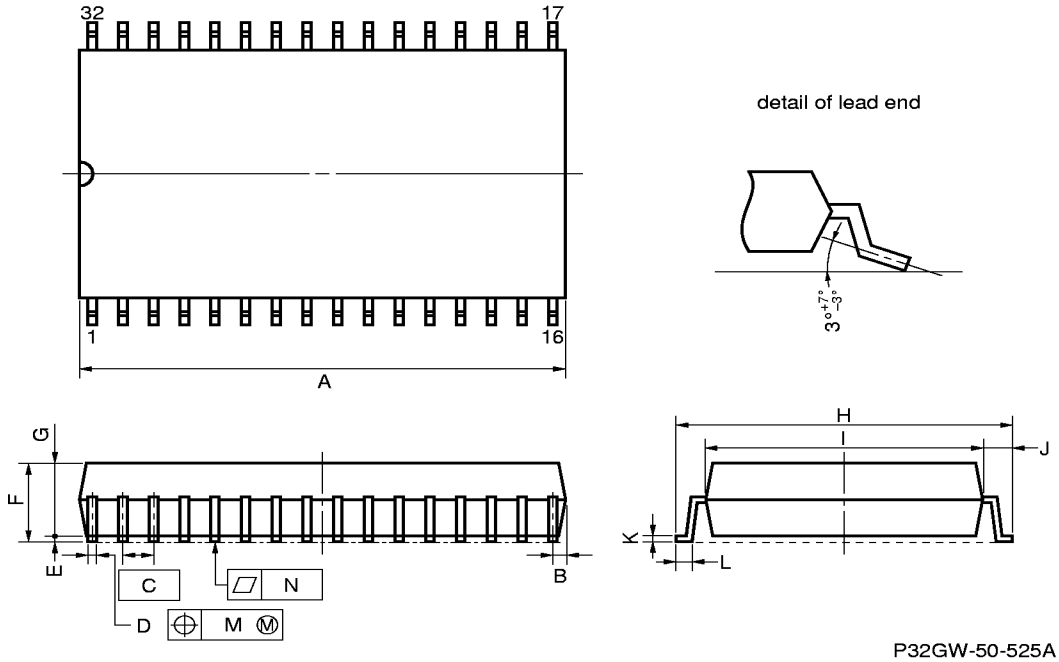


Note B version: 2.7 V, C version: 2.2 V, D version: 1.8 V

Remark The other pins (/CE1, Address, I/O, /WE, /OE) can be in high impedance state.

Package Drawings

★ **32 PIN PLASTIC SOP (525 mil)**



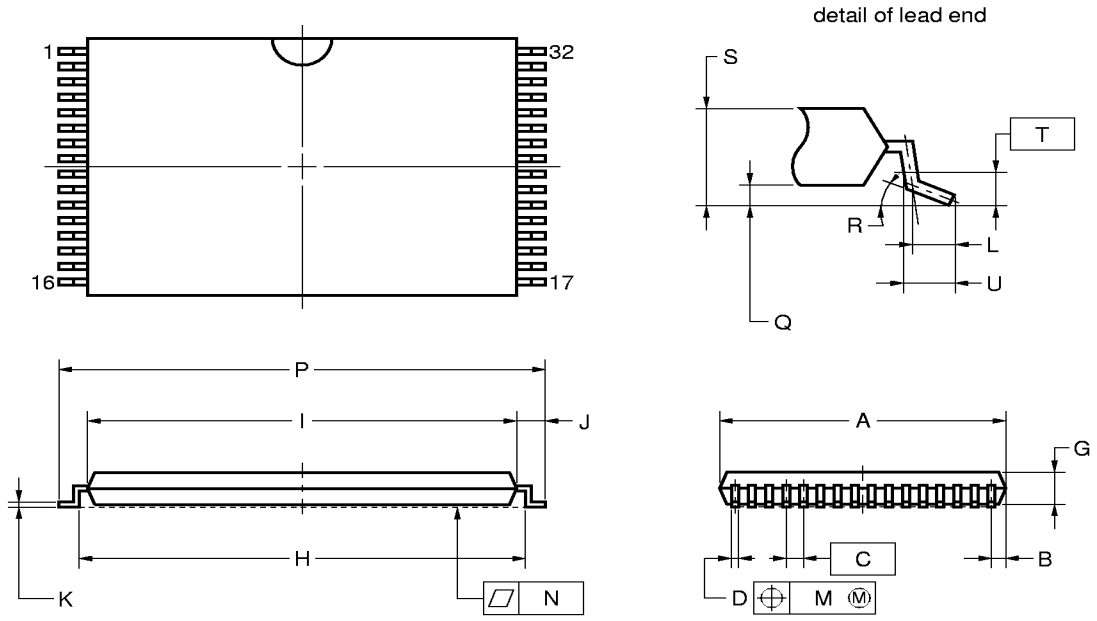
P32GW-50-525A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.61 MAX.	0.812 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.15±0.05	0.006
F	2.95 MAX.	0.117 MAX.
G	2.7	0.106
H	14.1±0.3	0.555±0.012
I	11.3	0.445
J	1.4±0.2	0.055±0.008
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.10	0.004

32PIN PLASTIC TSOP (I) (8x13.4)



NOTE

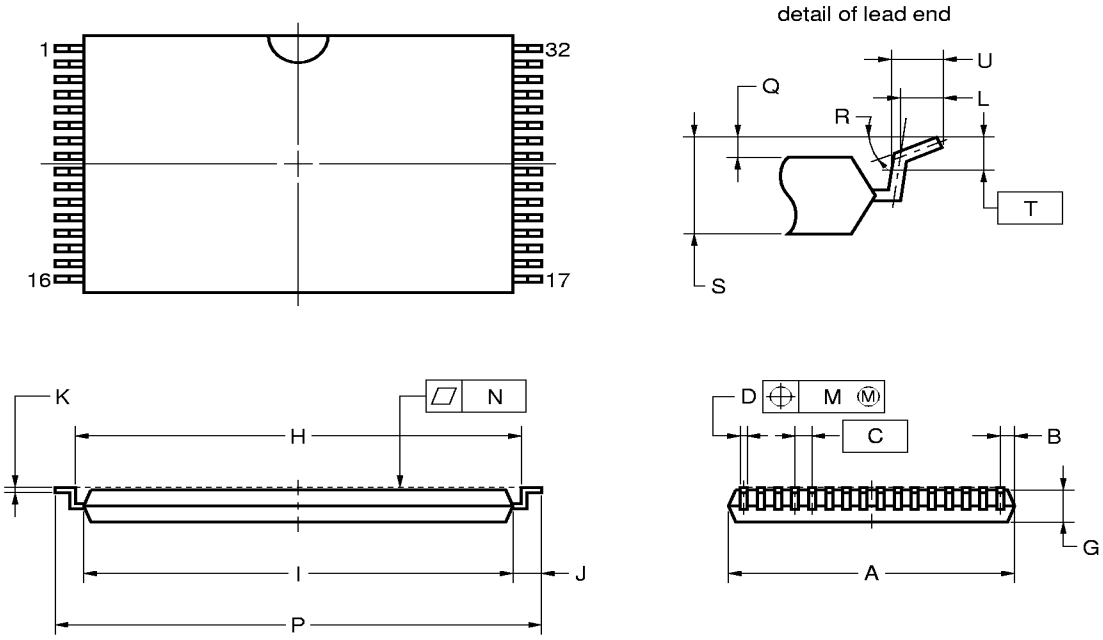
(1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

(2) "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX. <0.331 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	$0.009^{+0.002}_{-0.003}$
G	1.0±0.05	$0.039^{+0.003}_{-0.009}$
H	12.4±0.2	0.488±0.008
I	11.8±0.1	$0.465^{+0.004}_{-0.005}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5	0.020
M	0.08	0.003
N	0.08	0.003
P	13.4±0.2	$0.528^{+0.008}_{-0.009}$
Q	0.1±0.05	0.004±0.002
R	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.	0.048 MAX.
T	0.25	0.010
U	0.6±0.15	$0.024^{+0.006}_{-0.007}$

P32GU-50-9JH-1

32PIN PLASTIC TSOP (I) (8x13.4)



NOTE

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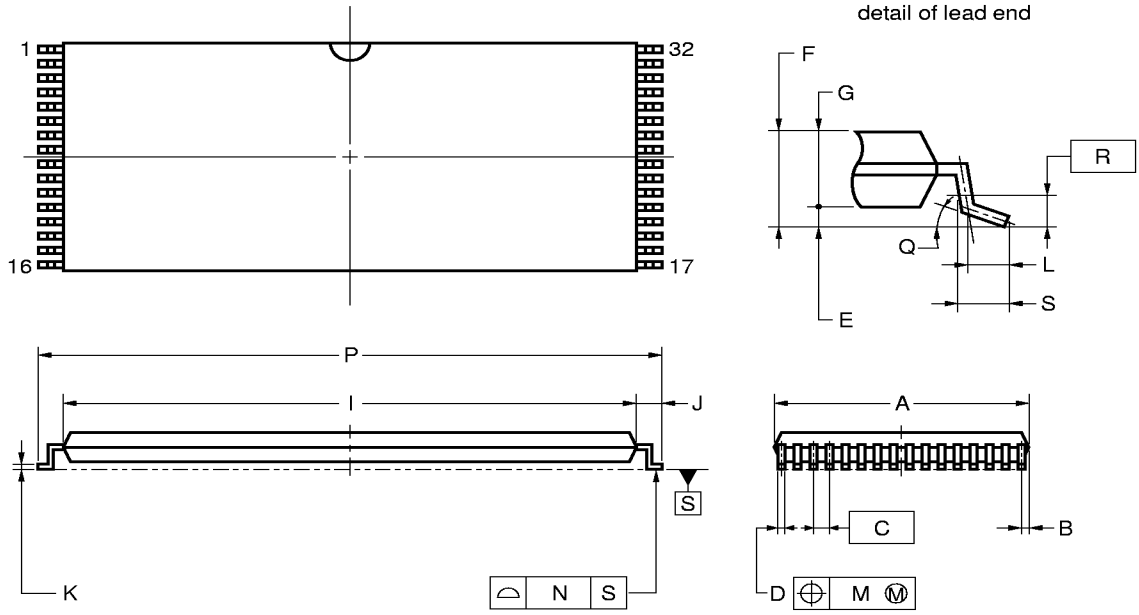
ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	$0.009^{+0.002}_{-0.003}$
G	1.0±0.05	$0.039^{+0.003}_{-0.009}$
H	12.4±0.2	0.488±0.008
I	11.8±0.1	$0.465^{+0.004}_{-0.005}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5	0.020
M	0.08	0.003
N	0.08	0.003
P	13.4±0.2	$0.528^{+0.008}_{-0.009}$
Q	0.1±0.05	0.004±0.002
R	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.	0.048 MAX.
T	0.25	0.010
U	0.6±0.15	$0.024^{+0.006}_{-0.007}$

P32GU-50-9KH-1

32 PIN PLASTIC TSOP (I) (8×20)



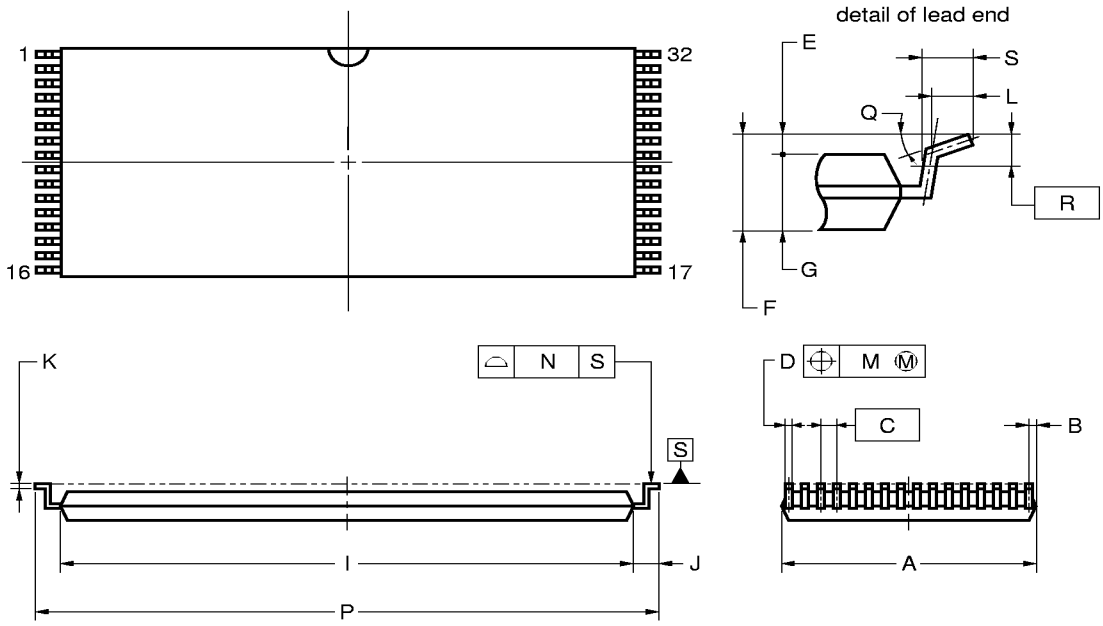
NOTES

1. Controlling dimension —— Millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX. <0.327 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	$0.009^{+0.002}_{-0.003}$
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97±0.08	$0.038^{+0.004}_{-0.003}$
I	18.4±0.1	$0.724^{+0.005}_{-0.004}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	0.145±0.05	$0.006^{+0.002}_{-0.003}$
L	0.5	0.020
M	0.10	0.004
N	0.10	0.004
P	20.0±0.2	$0.787^{+0.009}_{-0.008}$
Q	$3°^{+5°}_{-3°}$	$3°^{+5°}_{-3°}$
R	0.25	0.010
S	0.60±0.15	$0.024^{+0.006}_{-0.007}$

S32GZ-50-KJH1

32 PIN PLASTIC TSOP (I) (8×20)



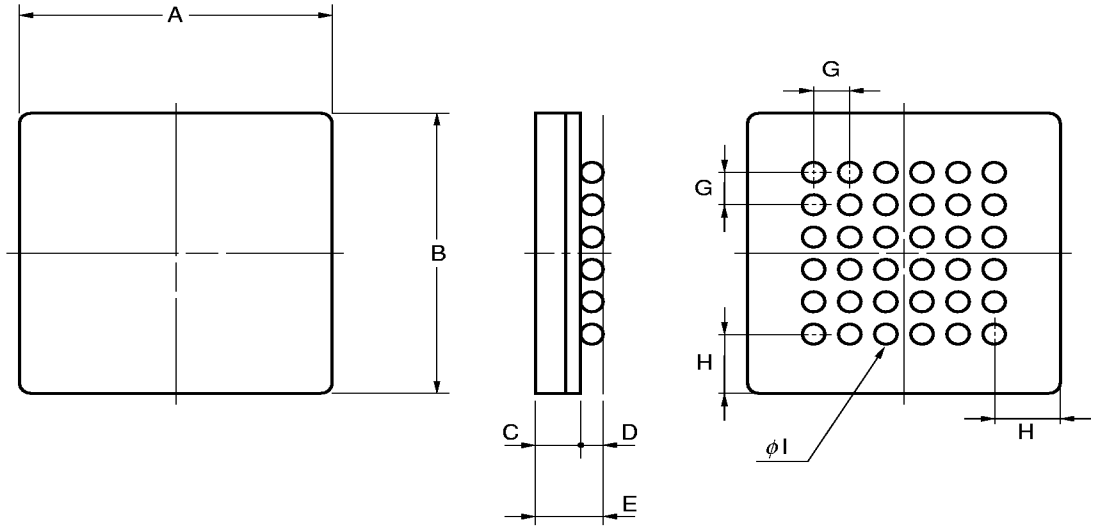
NOTES

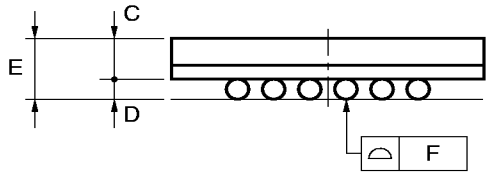
1. Controlling dimension —— Millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX. <0.327 inch MAX.>).

ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	$0.009^{+0.002}_{-0.003}$
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97±0.08	$0.038^{+0.004}_{-0.003}$
I	18.4±0.1	$0.724^{+0.005}_{-0.004}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	0.145±0.05	$0.006^{+0.002}_{-0.003}$
L	0.5	0.020
M	0.10	0.004
N	0.10	0.004
P	20.0±0.2	$0.787^{+0.009}_{-0.008}$
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25	0.010
S	0.60±0.15	$0.024^{+0.006}_{-0.007}$

S32GZ-50-KKH1

36 PIN PLASTIC-FPBGA (6.0 × 6.0)





ITEM	MILLIMETERS
A	6.0±0.1
B	6.0±0.1
C	0.68±0.1
D	0.3±0.05
E	1.1 MAX.
F	0.1
G	0.75±0.05
H	1.125
I	0.45±0.05

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD441000L-X.

Type of Surface Mount Device

★ μPD441000LGW-BX: 32-pin Plastic SOP (525 mil)
★ μPD441000LGW-CX: 32-pin Plastic SOP (525 mil)
★ μPD441000LGW-DX: 32-pin Plastic SOP (525 mil)
μPD441000LGU-BX-9JH: 32-pin Plastic TSOP (I) (8 x 13.4 mm) (Normal bent)
μPD441000LGU-BX-9KH: 32-pin Plastic TSOP (I) (8 x 13.4 mm) (Reverse bent)
μPD441000LGU-CX-9JH: 32-pin Plastic TSOP (I) (8 x 13.4 mm) (Normal bent)
μPD441000LGU-CX-9KH: 32-pin Plastic TSOP (I) (8 x 13.4 mm) (Reverse bent)
μPD441000LGU-DX-9JH: 32-pin Plastic TSOP (I) (8 x 13.4 mm) (Normal bent)
μPD441000LGU-DX-9KH: 32-pin Plastic TSOP (I) (8 x 13.4 mm) (Reverse bent)
μPD441000LGZ-BX-KJH: 32-pin Plastic TSOP (I) (8 x 20 mm) (Normal bent)
μPD441000LGZ-BX-KKH: 32-pin Plastic TSOP (I) (8 x 20 mm) (Reverse bent)
μPD441000LGZ-CX-KJH: 32-pin Plastic TSOP (I) (8 x 20 mm) (Normal bent)
μPD441000LGZ-CX-KKH: 32-pin Plastic TSOP (I) (8 x 20 mm) (Reverse bent)
μPD441000LGZ-DX-KJH: 32-pin Plastic TSOP (I) (8 x 20 mm) (Normal bent)
μPD441000LGZ-DX-KKH: 32-pin Plastic TSOP (I) (8 x 20 mm) (Reverse bent)
μPD441000LF1-BA1-BX: 36-pin Plastic FPBGA (6.0 x 6.0 mm)
μPD441000LF1-BA1-CX: 36-pin Plastic FPBGA (6.0 x 6.0 mm)
μPD441000LF1-BA1-DX: 36-pin Plastic FPBGA (6.0 x 6.0 mm)